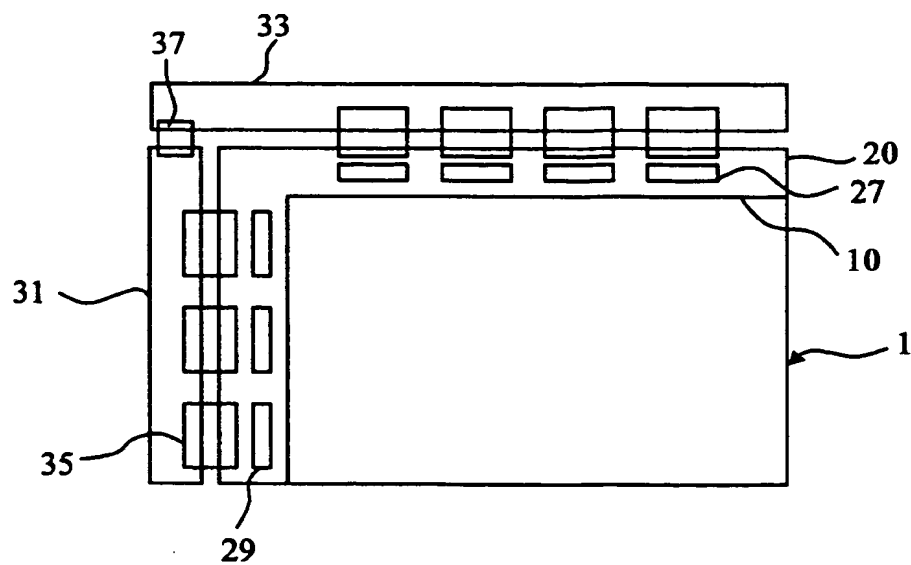
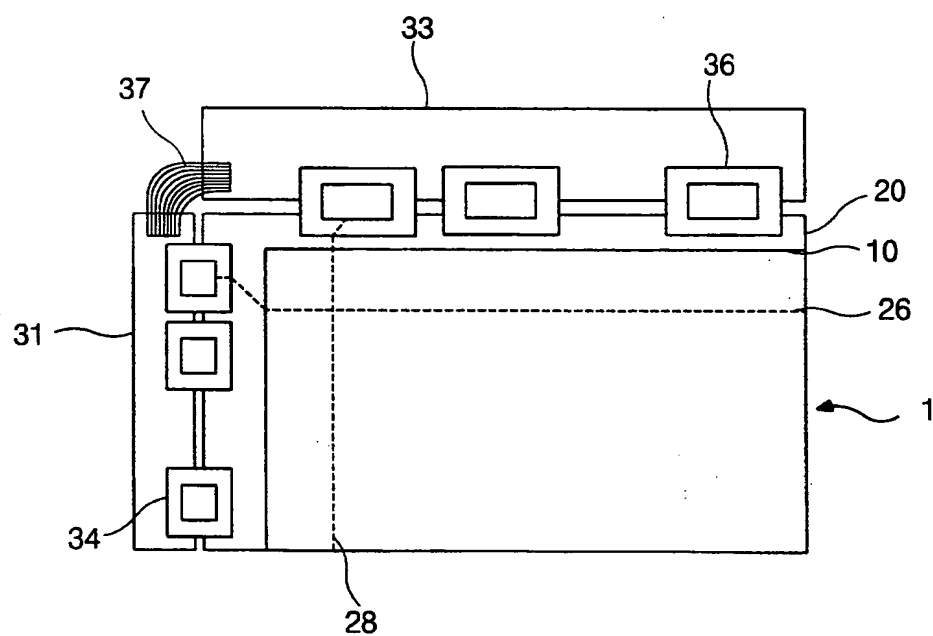




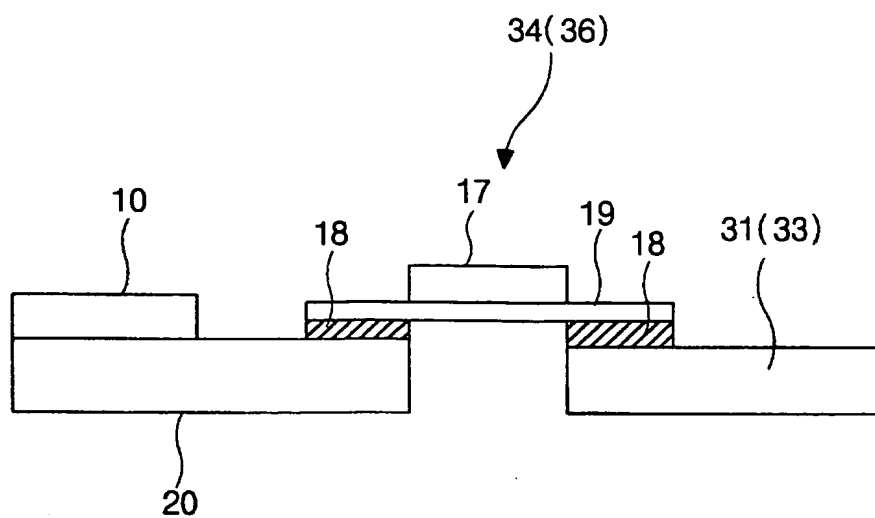
FIG 1



(related art)
FIG. 2



(related art)
FIG. 3



(related art)
FIG. 4

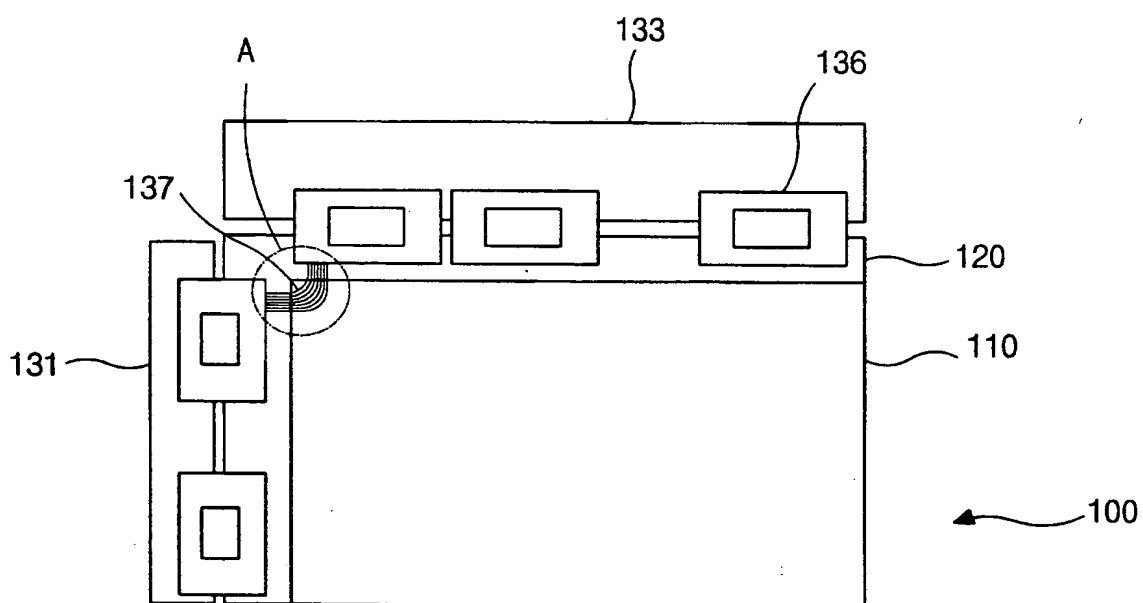


FIG 5

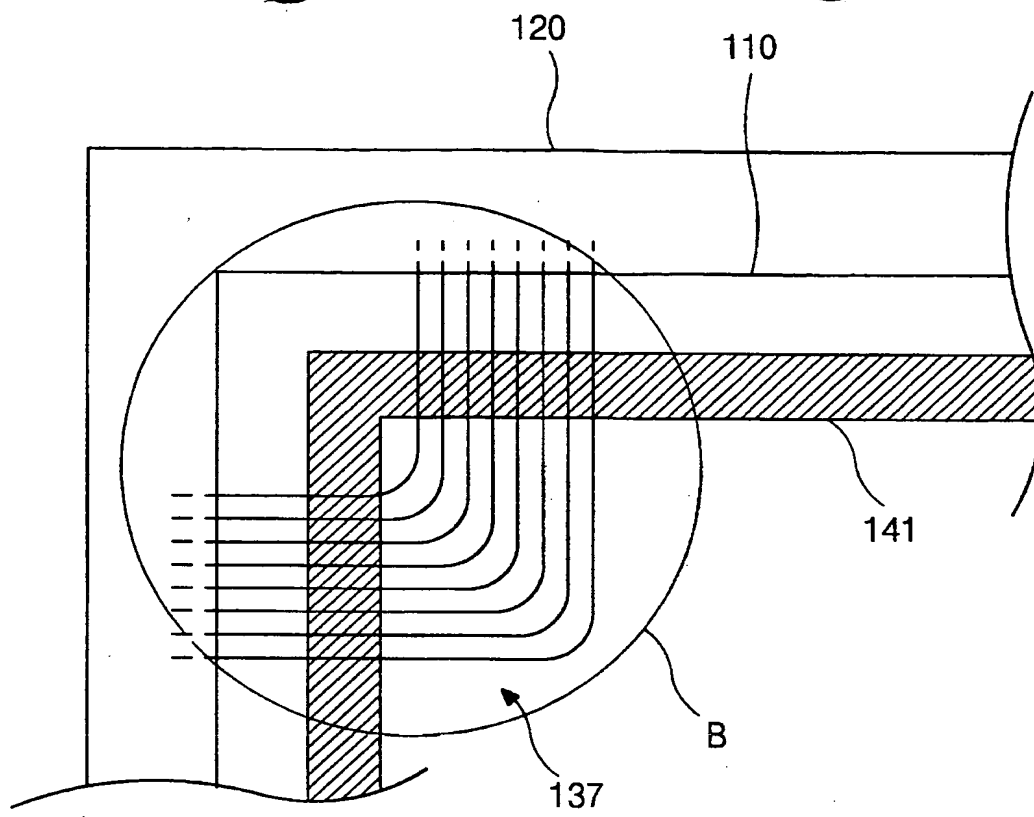
[illegible]

FIG. 6



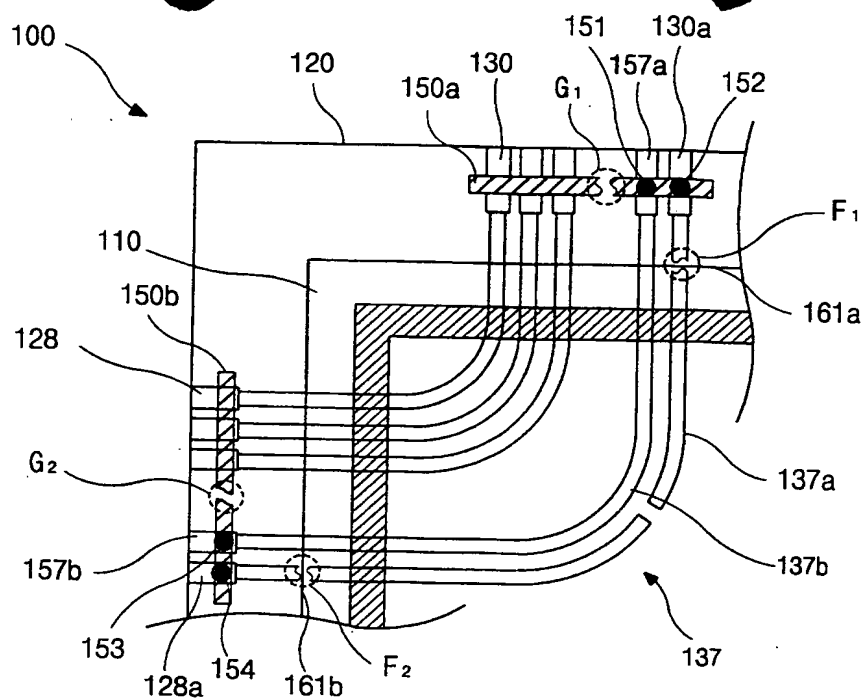


FIG 9

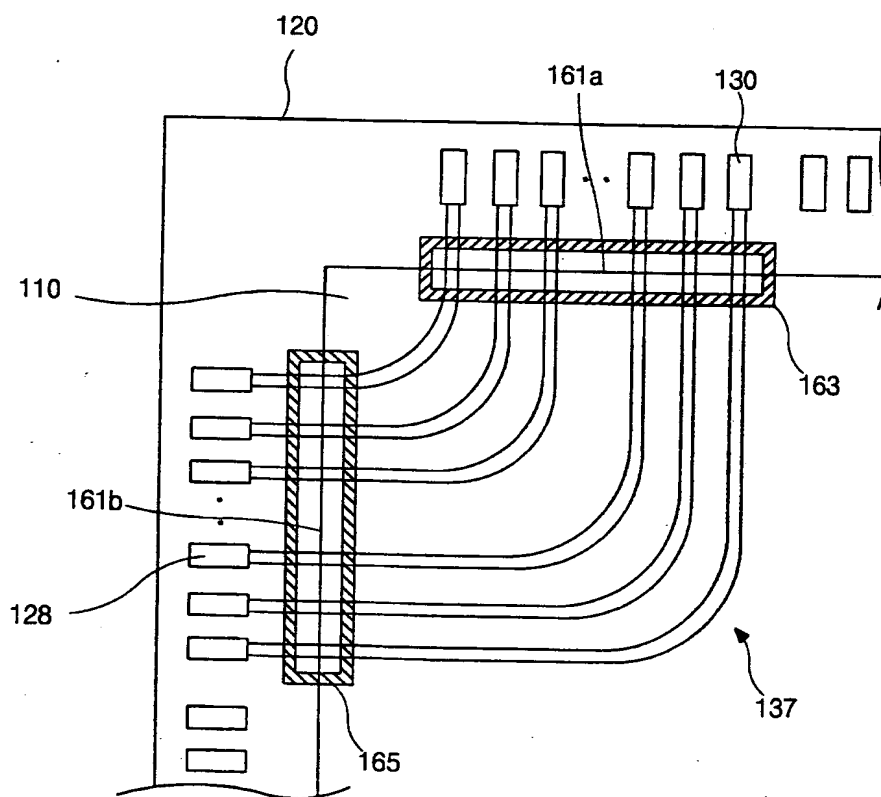


FIG 10A

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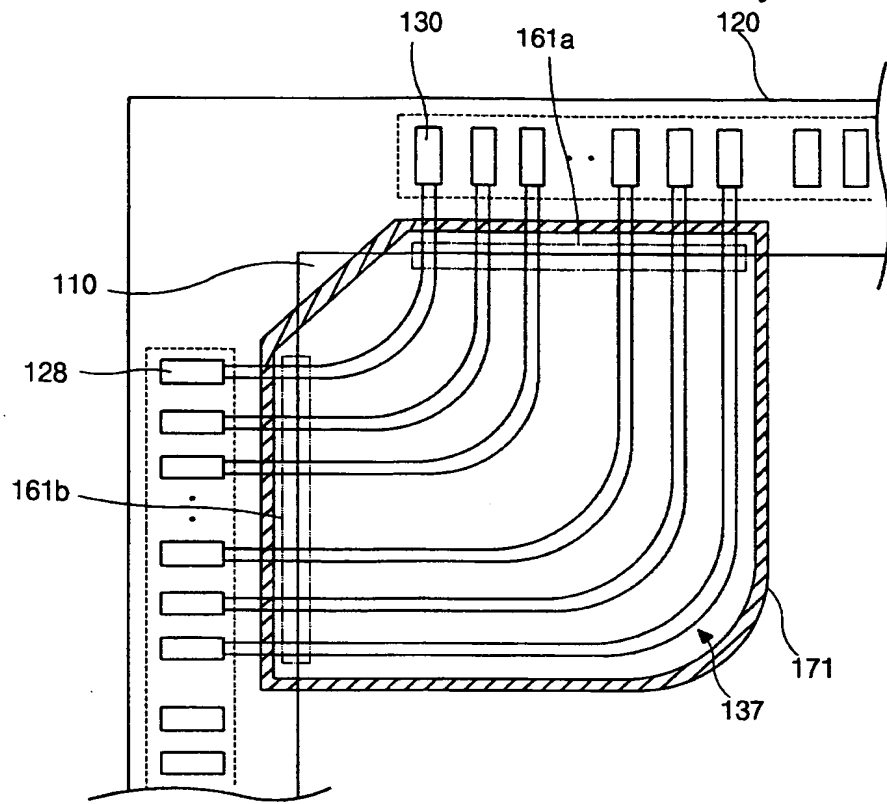


FIG 11A

FIG. 11B

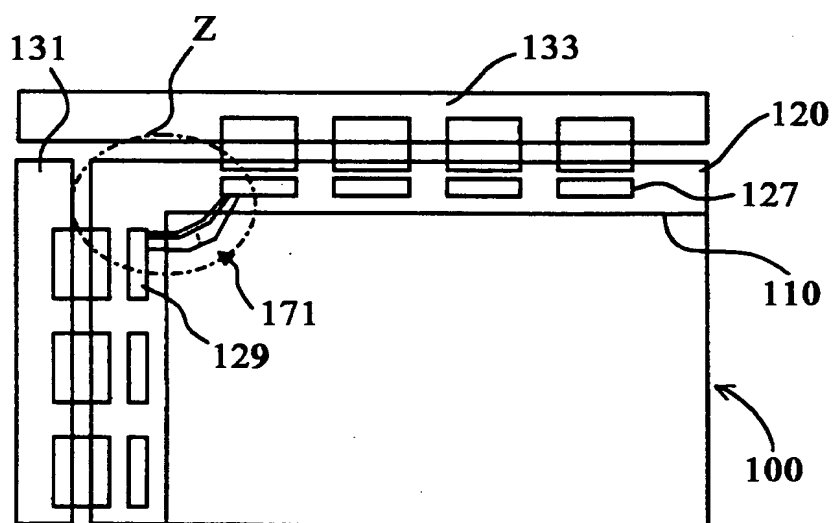


FIG 12

A schematic diagram showing a cross-sectional view of a semiconductor device. The diagram includes a substrate 110 with a top layer 120. Within layer 120, there are several rectangular conductive regions 130. Below layer 120, there are interconnect layers 125 and 126. Vertical vias 137 connect the regions in layer 120 to those in layer 126. Specific labels include 161a pointing to a region in layer 120, 161b pointing to a region in layer 126, and 137c pointing to a via. Dashed boxes highlight certain areas of the structure.

FIG 13B

FIG 14

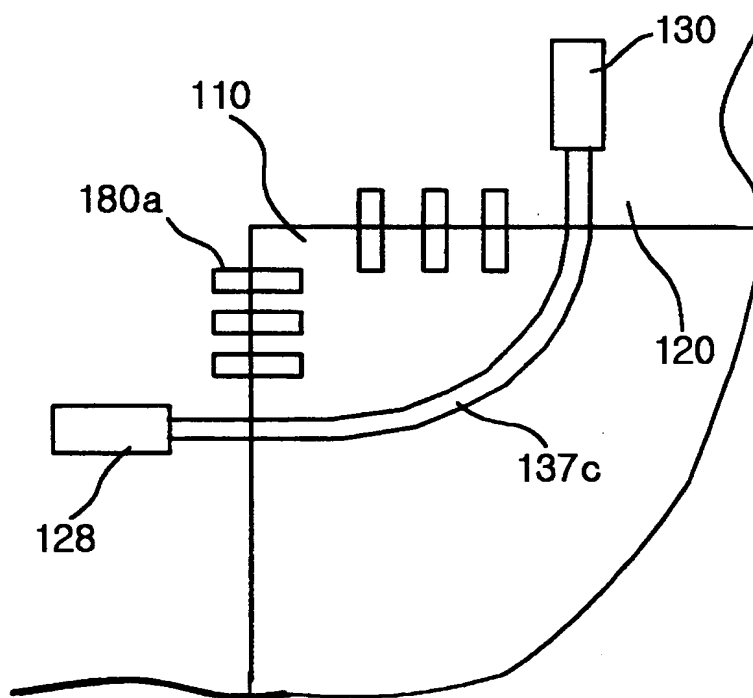


Diagram illustrating a system architecture. A central unit 110 is connected to a storage unit 128 and a display unit 130 via a bus 120. A control unit 180b is also connected to the bus 120. The diagram shows a central unit 110, a storage unit 128, a display unit 130, and a control unit 180b, all connected to a common bus 120. A control unit 137c is also shown connected to the bus 120.

This cross-sectional view shows a substrate 120 with a thin layer 190 on top. A series of gate structures 137 are formed on the surface, each consisting of a gate dielectric 137a and a gate electrode 137c. The gate structures are separated by spacers 180b. The entire structure is covered by a passivation layer 192. The cross-section is taken along line XVI-XVI.

FIG. 16A

